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THE CALIBRATION OF A UNIVERSAL TEST FIXTURE

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ABSTRACT

A broadband, universal transistor test fixture uses exchangeable inserts to accommodate most transistor types. The calibration of the fixture and its inserts by a reliable, accurate and easy to use scheme is described.

INTRODUCTION

Many schemes have been proposed for the measurement of the parameters of microwave active devices. Although a universal test fixture for microwave transistors which accommodates a wide range of package styles is not, in principle, difficult to realize; the key to a viable measurement lies in the technique used for calibration. This determines the ease and accuracy of the subsequent process of de-embedding the transistor parameters from the measurement at the external connectors. The fixture described in this paper offers a device which, it is hoped, meets the full range of requirements for frequency coverage, device types, low loss (especially important for noise measurements) and a fully defined, systematic calibration procedure.

The universal transistor test fixture has been developed from a proven design[1] and the present contribution describes and analyzes the calibration, verification and de-embedding techniques which ensure that the fixture can be used to provide accurate results for a wide range of transistor package styles at frequencies up to 18 GHz. It is assumed that an automatic network analyzer is used for the measurement of S-parameters and the problem then becomes one of calibration to determine the parameters of the network in which the device to be tested is embedded.

THE FIXTURE

The basic principles of the fixture design are shown in Figure 1. The permanent outer sections of the fixture are in 7mm air line and connections to the network analyzer are by means of APC-7 connectors. The fixture is assembled with a two part insert sandwiched between the outer sections. The insert is the item which customizes the fixture for a particular transistor style. Once assembled, the top section of the fixture serves as a hinged lid which allows rapid and repeatable insertions of transistors. The inner conductors of the 7mm lines are slotted to accommodate the transistor input and output lead which are held in place by 0.04" diameter plastic rods. In order to ensure a repeatable contact, there is a small lip at the end of the co-axial line inner conductors.

CALIBRATION

The calibration problem has three distinct aspects[2];

(1) System calibration - determination of the systematic errors of the network analyzer system and those fixed components which are independent of the device to be tested. In practice this needs to be repeated each time the system is used and a reference plane as close to the device under test as possible should be employed. The overall measurement circuit is shown in Figure 2. The scheme used in this application calibrates at a reference plane within the fixture and includes all the permanent components of the test fixture in the ANA 12-term error model[3].

The ANA system calibration requires the fixture to be split apart and four components inserted in place of the device insert.

(a) Double fixed load (VSWR <1.05 to 18 GHz)
(b) Double fixed short circuit
(c) Double shield open
(d) Thru.

These components are derived from 7mm co-axial types but have the advantage of providing the necessary measurements for the error model with few manual operations. It should be noted that the double load allows both directivity and isolation at both ports to be evaluated. The length and loss of the thru are accounted for in the calibration software. The fixture is re-assembled with the insert in place and is then ready for use.

(2) Insert Calibration - The presence of the insert to customize the fixture to a particular package style results in a discontinuity which must be represented by an additional network between the measurement plane determined in the system calibration and the device under test. The circuit model is shown in Figure 3.

Whilst the discontinuity is assumed to be characterized by a pi-network (three parameters), the validity of this assumption can be confirmed to some extent by the measurements. After system calibration, three novel artifacts are measured to evaluate the three quantities. The devices are:

1. A short circuit insert made entirely of one piece of gold plated brass and accurately defining the plane of the device to be tested;
2. An open circuit insert to charactize the residual transistor leads; and
3. An insert with a thru connection of virtually zero electrical length intended to charactize the reduced aperture in which the transistor is located.

A simple way to obtain the parameters is to use the first two sets of data to obtain estimates for the values and then curve fit using the third. The following description uses data obtained from measurements on a 70mil microstrip package (NEC-type 83).

1. The short circuit insert is shown schematically in Figure 4. The input impedance of this network is

$$Z_1 = \frac{jwL}{1-w^2LC_1} \quad (1)$$

which, at low frequencies is approximately jwL.

The reflection measurements show a phase slope of approximately 5^0/GHz for frequencies below 10 GHz, yielding a value for L of approximately 0.35 nH.

2. The open circuits are shown schematically in Figure 5. The impedance is

$$Z_2 = \frac{1-w^2LC_2}{jw(C_1+C_2-w^2LC_1C_2)} \quad (2)$$

At low frequencies, this approximates to

$$Z_2 = \frac{1}{jw(C_1+C_2)}$$

and from the phase slope of the reflection coefficient.

$$(C_1+C_2) \simeq 0.17\,pF$$

By extrapolation, the data suggests a series resonance at approximately 35GHz giving a value of 0.06 pF for C_2 from equation (2) and hence a value of .11 pF for C_1.

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3. The thin thru insert is shown schematically in Figure 6. A typical set of results are shown in Figure 7. Using the estimated values for C_1, C_2 and L obtained in the earlier part of the procedure, the equivalent circuit of Figure 6 is fitted to the measured data. The results yield C_1 = 0.112 pF, C_2 = 0.055 pF, L = 0.395 nH. Further optimization exercises, using the data obtained in the short circuit, open circuit and thru circuit (6 sets of data) result in C_1 = 0.067 pF, C_2 = 0.055 pF, L = 0.367 nH. These results indicate that the model is self-consistent and appears to be a reasonably good approximation over the frequency range 2-18 GHz. It should be noted that the insert calibration and associated calculations need be carried out only once for each insert and the element values obtained are used in the de-embedding process after system calibration.

(3) Verification - The use of a circuit model in the de-embedding process, the complexity of the system and the possibility of incorrect assembly, make it essential to be able to check that the calibration has been carried out correctly. This is achieved by means of simple check devices, independent of the devices used for calibration. The form of these devices is immaterial, at present they comprise a planar short and planar thru (Figure 8) made of 8mil thick gold-plated material.

Measurements of these devices and comparison with their known properties (Figures 9 & 10) provides confirmation of the validity of the calibration and de-embedding as well as monitoring the longer term stability and repeatability of the test fixture.

DE-EMBEDDING

The S-parameters of the transistor and the insert are obtained after measurements and application of the 12-term error correction calculations $[S_{meas}]$. The process of de-embedding the transistor S-parameters from the insert is then:

. Convert $[S_{meas}]$ to $[T_{meas}]$ (transfer scattering matrix)

. Set up the T-matrix for the pi networks $[T_{pi1}]$, $[T_{pi2}]$ from $(-C_2, -L, -C_1)$ and $(-C_1, -L, -C_2)$

. Cascade the three T-matrices $[T_{pi1}][T_{meas}][T_{pi2}]$

. Convert the resultant T-matrix to yield the S-matrix of the transistor alone.

CONCLUSIONS

The detailed procedure for the calibration process of a universal transistor test fixture has been demonstrated and shown to be simple, reliable and self-consistent. The principle features are:

(a) A set of standards to provide for the system calibration of an automatic network analyzer with a fixture attached;

(b) Suitable devices and a scheme for deriving a circuit model for the presence of an insert to customize the fixture for a particular package style;

(c) A technique for de-embedding the transistor S-parameters from the measurements; and

(d) A means of verification that the procedure has been carried out correctly.

ACKNOWLEDGEMENTS

One of the authors (RDP) gratefully acknowledges support received from Hewlett-Packard (Santa Rosa) during sabbatical leave from The University of Leeds. Thanks are also due for the contributions of colleagues at California Eastern Laboratories, Hewlett-Packard and Maury Microwave Corporation.

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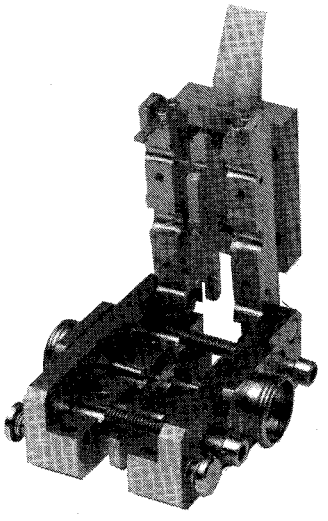

Fig.1

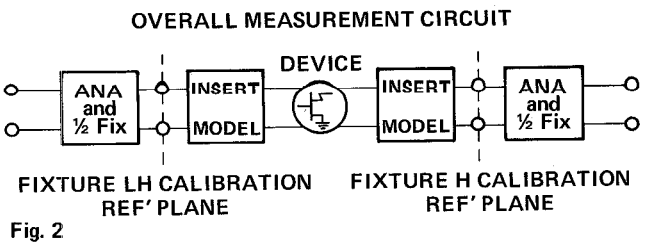

Fig. 2

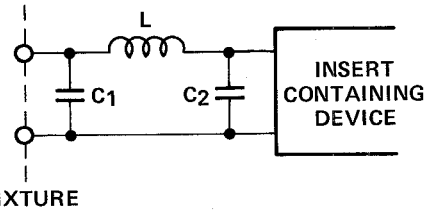

Fig. 3

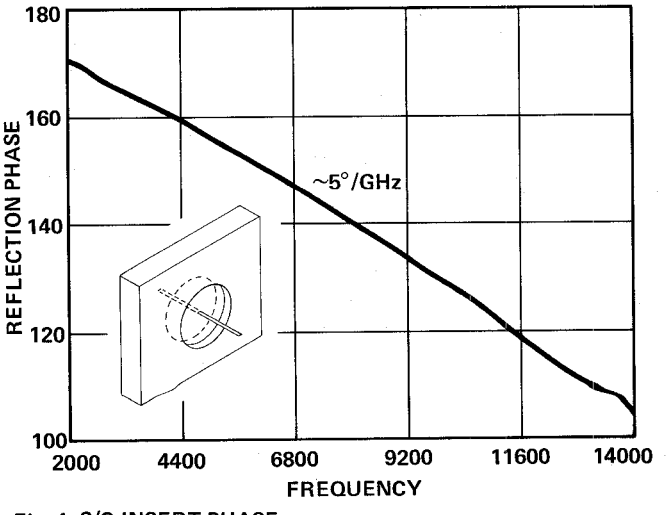

Fig. 4 S/C INSERT PHASE

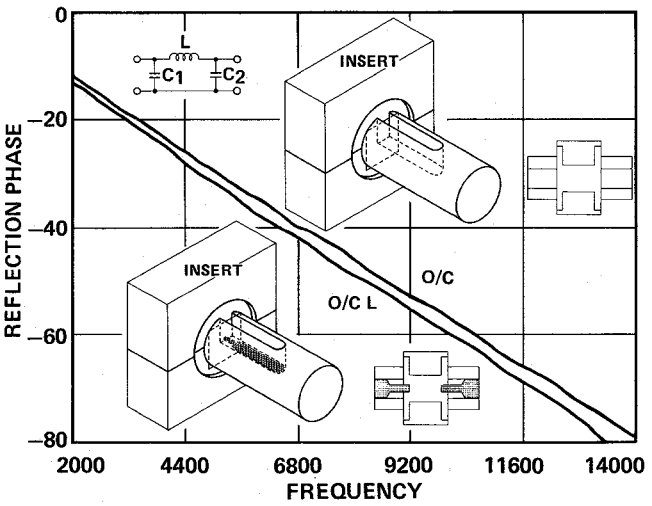

Fig. 5 O/C AND O/C L PHASE

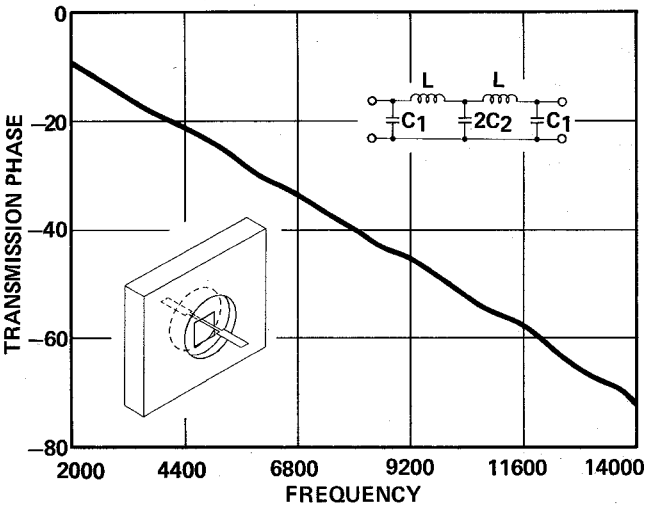

Fig. 6 THIN THRU INSERT PHASE

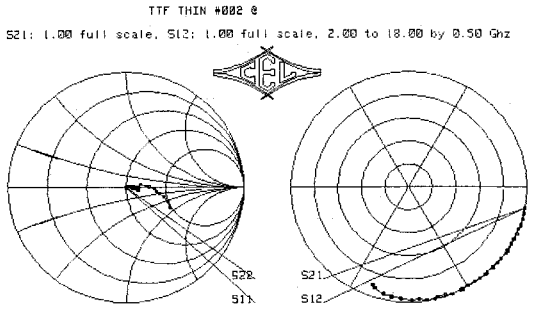

Fig. 7

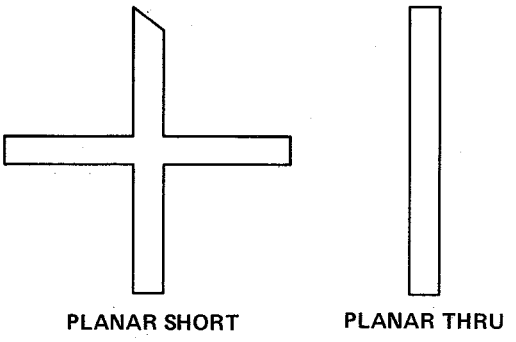

Fig. 8

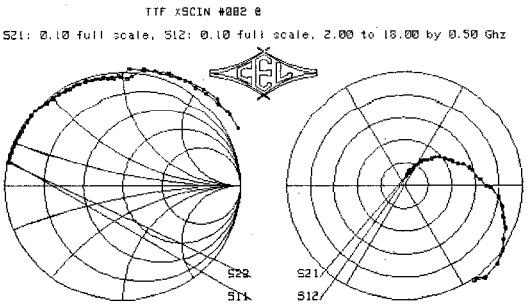

Fig. 9

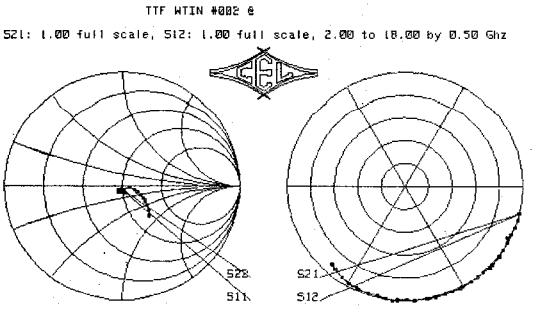

Fig. 10